

# Energy-Efficient Memories using Magneto-Electric Switching of Ferromagnets

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**Abstract**—Voltage driven magneto-electric (ME) switching of ferro-magnets has shown potential for future low-energy spintronic memories. In this paper, we first analyze two different ME devices *viz.* ME-MTJ and ME-XNOR device with respect to writability, readability and switching speed. Our analysis is based on a coupled magnetization dynamics and electron transport model. Subsequently, we show that the decoupled read/write path of ME-MTJs can be utilized to construct an energy-efficient dual port memory. Further, we also propose a novel content addressable memory (CAM) exploiting the compact XNOR operation enabled by ME-XNOR device.

**Index Terms**—Magneto-electric effect, CAM, dual port, memory, XNOR, LLG.

## I. INTRODUCTION

MAGNETO-RESISTIVE memories based on current driven Spin Transfer Torque (STT) [1], have attracted immense research interest due to their non-volatility, almost unlimited endurance and area-efficiency [2]. However, STT based memories suffer from inherent low switching speed and high write-energy consumption [3]. Recently, voltage induced Magneto-Electric (ME) effect, has shown potential for fast and energy-efficient switching of ferromagnets [4].

Many device proposals for memory [5], [6] and logic applications [7]–[9] of the ME effect can be found in the literature. In this paper, we explore two different ME devices - i) ME magnetic tunnel junctions (ME-MTJs) [7] and ii) ME-XNOR device [7], [9]. We analyze the ME devices with respect to writability, readability and switching speed using a coupled magnetization dynamics and transport model. Further, we propose two novel energy-efficient memories - i) a dual port memory and ii) a content addressable memory (CAM), using the aforementioned ME devices.

## II. ME EFFECT

Various single phase [10] and composite multi-ferroic materials [11] have been experimentally demonstrated to exhibit the ME effect. ME effect is due to exchange bias coupling in single phase materials [12] and is usually due to strain coupling [11] in case of composite materials. For example, in single phase  $\text{BiFeO}_3$  due to the coupling between the ferroelectric polarization, the (anti) ferromagnetism of  $\text{BiFeO}_3$ , and the ferromagnetism of an underlying nano-magnet, the magnetization of the nano-magnet can be switched by application of

an electric field [13]. Similarly, strain coupled magnetization reversal in PMN-PT has been proposed in [11].

Note, since multi-ferroics in general and ME effect in particular, is currently an area of intense research investigation, we do not follow a particular material set or experiment. Rather, in this work, we treat the ME effect by a generic parameter referred to as the magneto-electric co-efficient ( $\alpha_{ME}$ ) [8], [9], [13] (explained later in the manuscript). Such an abstraction of the ME effect is justified, since the aim of the present paper is not to explore the various physical phenomena driving the ME effect. Instead we intend to examine the implications of ME based devices with focus on memory applications.

## III. ME DEVICES UNDER CONSIDERATION

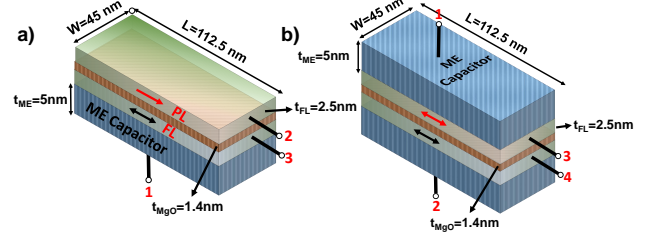


Fig. 1. (a) Schematic of the ME-MTJ and (b) ME-XNOR. We have assumed  $M_S = 1257.3 \text{ K A/m}$  [14],  $\alpha = 0.1$ ,  $K_i = 1 \text{ mJ/m}^2$  [14],  $\alpha_{ME} = 1/c \text{ m s}^{-1}$ , where  $c$  is speed of light,  $\epsilon_{ME} = 500$  [8],  $T = 300 \text{ K}$ .

We consider two ME based devices – ME-MTJ [7] and ME-XNOR [7], [9], with focus on memory applications. ME-MTJ consists of an MTJ in contact with an ME oxide underlayer as shown in Fig. 1(a). The MTJ itself is composed of a *pinned layer* (PL), a *free layer* (FL) and an oxide spacer (usually MgO [15]). Depending on the orientations of the free and the pinned layer the ME-MTJ can be in either low resistance parallel (P) state or high resistance anti-parallel (AP) state. The normalized difference in the resistances of the AP and P state is expressed by the tunnel magneto-resistance (TMR) ratio of the MTJ.

In order to switch the ME-MTJ from P (AP) to AP (P) state a positive (negative) voltage exceeding a certain threshold needs to be applied on terminal 1 in Fig. 1(a). The metal contact to the ME oxide, the ME oxide itself and the free layer of the MTJ can be considered as a capacitor. On the other hand, the value stored in the ME-MTJ can be read by sensing the resistance between terminals 1 and 2.

In Fig. 1(b) we show the ME-XNOR device. The ME-XNOR device consists of two free layers separated by MgO and in contact with respective ME oxides. If the voltage polarity on the terminals 1 and 2 are the same, the MTJ stack would be in P state (measured between terminals 3 and 4), while a different voltage polarity on the two terminals would lead to an AP state. Thus, the proposed device emulates an

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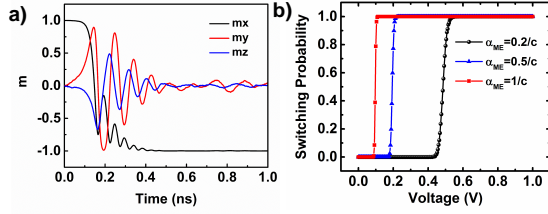


Fig. 2. (a) Magnetization dynamics. (b) Switching probability versus voltage.

XNOR functionality. ME-XNOR device in previous works have been used for logic applications [9]. In this work, we would later show that ME-XNOR device can be used to construct an energy efficient CAM. In the next section, we describe the simulation model.

#### IV. DEVICE MODELING

Under mono-domain approximation, magnetization dynamics can be modeled using the LLG equation, proposed by Landau, Lifshitz and Gilbert, as shown below [16], [17]

$$\frac{\partial \hat{m}}{\partial t} = -|\gamma| \hat{m} \times H_{EFF} + \alpha \hat{m} \times \frac{\partial \hat{m}}{\partial t} \quad (1)$$

where  $H_{EFF}$  is the effective magnetic field.  $H_{EFF}$  is the sum of the demagnetization field [18], [19], the interface anisotropy field [3] and any other external field.  $\hat{m}$  is the unit magnetization vector,  $\gamma$  is the gyromagnetic ratio and  $\alpha$  is the Gilbert damping constant. The thermal noise is modeled using the Brown's model [20] and is accounted for by expressing a contributing field to  $H_{EFF}$  as  $\vec{H}_{thermal} = \zeta \sqrt{\frac{2\alpha kT}{|\gamma| M_S V dt}}$ , where  $\zeta$  is a vector with components that are zero mean Gaussian random variables with standard deviation of 1.  $V$  is volume of the free layer,  $T$  is the temperature and  $k$  is the Boltzmann's constant and  $dt$  is time step. The ME effect can be included in  $H_{EFF}$  by writing the ME field as [8]  $H_{ME} = \frac{1}{\mu_0} \alpha_{ME} E = \frac{1}{\mu_0} \alpha_{ME} \frac{V_{ME}}{t_{ME}}$ , where the magneto-electric constant is  $\alpha_{ME}$  [21],  $E$  is the electric field and  $V_{ME}$  is the voltage across the ME capacitor.

Equation (1) can be solved numerically through the Heun's method [22]. In addition, we used the Non Equilibrium Green's Function (NEGF) formalism [23] for estimation of the resistance of the MTJ stack.

#### V. DEVICE CHARACTERISTICS

##### A. Writability

Writing into ME devices is accomplished by application of appropriate voltages across the ME capacitor. An important parameter that dictates the write voltage and hence the write energy is the magneto-electric co-efficient ( $\alpha_{ME}$ ).  $\alpha_{ME}$  is the ratio of magnetic field generated per unit applied electric field [13]. Experimentally, various ME materials have shown  $\alpha_{ME}$  in the range  $0.1/c$  to  $1/c$  ( $c$  is speed of light) [21]. In Fig. 2 (a), we show a typical magnetization switching curve and in Fig. 2 (b) we plot the switching probability as a function of voltage across the ME capacitor for different values of  $\alpha_{ME}$ . It can be seen, ME materials with high  $\alpha_{ME}$  are desirable for achieving low write energy.

##### B. Readability

In a memory configuration, a CMOS transistor is used in series with the storage device. Therefore, the bit-cell TMR *i.e.* the TMR of the device with the series resistance of the CMOS transistor is a more relevant metric for the sensing margin as opposed to the device TMR. In Fig. 3(a), we have shown the

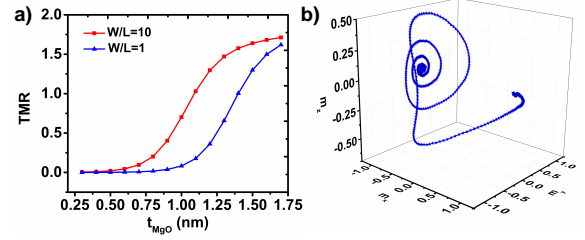


Fig. 3. (a) TMR versus MgO thickness (b) A typical 3D switching trajectory

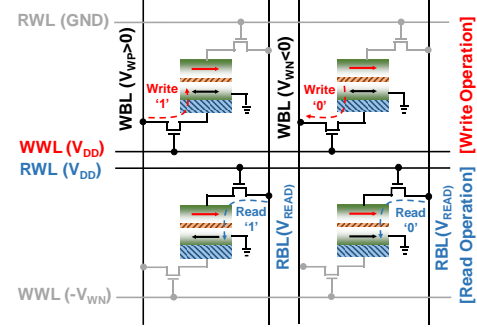


Fig. 4. Dual port memory using decoupled read/write path of ME-MTJs

bit-cell TMR as a function of MgO thickness assuming a 45nm PTM [24] transistor in series with varying W/L (width/length) ratios. It can be seen a higher value of MgO thickness is required to increase the bit-cell TMR and reduce the parasitic effect of the transistor series resistance [3], [25]. For the ME devices, due to the decoupled read/write paths, the thickness of the MgO oxide can be increased without degrading the write efficiency (which is dictated by the ME oxide). Thus, the decoupled read/write paths for ME devices allows for better sensing due to increased bit-cell TMR.

##### C. Switching Speed

Though, a detailed switching dynamics for ME devices is still under research investigation [13], yet it is expected that ME switching would be much faster as compared to STT switching [21]. This is because ME switching dynamics behaves as if the magnetization direction is being switched by an external field which does not require an incubation delay [26] to initiate the switching process. In Fig. 3(b) we have shown a typical 3D trajectory of the ME switching mechanism, based on the model presented in section IV. It can be seen if the applied electric field is strong enough, the magnetization vector starts switching without any initial incubation delay. In our simulations for an  $\alpha_{ME}$  of  $1/c$ , complete reversal was obtained within 500ps.

#### VI. ME MEMORY DESIGN

##### A. ME Dual Port Memory

The proposed dual port memory using ME-MTJs is shown in Fig. 4. Each bit-cell consists of one ME-MTJ and two transistors. The transistor connected to WWLs are the write transistors and those connected to RWLs are the read transistors. Data can be written into the ME-MTJs by activating the write transistors of a particular row and applying appropriate write voltages (positive or negative) on WBLs. Similarly, for reading out the data, the read transistors of a given row are activated and a read voltage is applied on RBLs. The current flowing through the bit-cell is then compared with a reference to sense the current state of the ME-MTJ.

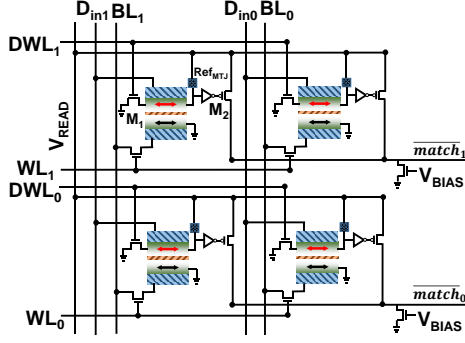


Fig. 5. Proposed CAM based on ME-XNOR device.

A dual port memory is characterized by simultaneous read and write operations *i.e.* while one row of the memory array is being read simultaneously another row of the memory array can be written into, thereby, improving the memory throughput [27]. The dual port nature of the proposed ME-MTJ memory can be explained as follows.

Let us consider row-1 in Fig. 4 is being written into. The write transistors corresponding to row-1 would be activated and by application of proper voltages on WBLs, a P or an AP state can be written into the ME-MTJs. Simultaneously, the read transistors corresponding to row-2 are activated and by sensing the current flowing through the RBLs, the state of the ME-MTJs connected to row-2 can be sensed. Our simulations indicate, write energy consumption per bit of 0.072 fJ for  $\alpha_{ME} = 1/c$  and read energy consumption of 1.3fJ for read voltage of 200mV and read time of 0.5ns. For the present proposal ME switching enables two orders of magnitude improvement in write energy and 8x improvement in switching speed as compared to STT based MTJs [28], in addition to improved TMR and throughput.

### B. ME CAM

The ME-XNOR based CAM cell is shown in Fig. 5 (a). The function of M1 is to selectively provide the ME-oxide capacitor with a ground connection when Data Input Line ( $D_{in}$ ) is activated. In the read circuit, a reference MTJ ( $Ref_{MTJ}$ ) forms a voltage divider with the resistance of the MTJ ( $R_{MTJ}$ ). The match signal is obtained at the drain of p-MOS M2 (denoted by node  $\overline{match}$ ), where a low voltage indicates a match is obtained and *vice-versa*. The node  $\overline{match}$  is pre-charged to  $V_{DD}$ . The strengths of the n-MOS and the p-MOS transistors, connected to the  $\overline{match}$  line, are adjusted such that even one activated p-MOS in a row is enough to maintain the output node in its pre-charged state.

The operation of the circuit can be divided into three modes: i) Write Mode, ii) Data Input Mode and iii) Read Mode. To write data in the lower (upper) ferromagnet, a write pulse corresponding to bit '1' (positive voltage) and '0' (negative voltage), respectively, is applied on the BL ( $D_{in}$ ) with the WL (DWL) activated. If the digital bit written in the lower ferromagnet is same as the data to be matched (stored in the upper ferromagnet), the MTJ switches to low resistance state. Finally in the *read mode*, a read pulse of 1 V ( $V_{READ}$ ) is applied for the read process. The output of the inverter goes 'high' only if the MTJ is in low resistance state indicating that the bit written in the top magnet in mode (ii) matches the bit stored in the bottom magnet. Matching of all bits in a row

turns all the p-MOS OFF and  $\overline{match}$  goes low, indicating that a match is found. The write and read energy per bit was found to be 0.072 fJ and 15 fJ, respectively, indicating two orders of magnitude improvement in write energy and comparable read energy as compared to previous works as in [29].

### VII. CONCLUSION

The prospects of achieving voltage driven switching of magnetization has renewed the interest for future low-power non-volatile spintronic memories. In this paper, we first analyze the writability, readability and switching speed of devices based on ME effect. Further, we propose two energy efficient memories using the ME devices. The proposed dual port memory allows for energy-efficient write operations in addition to faster speed, improved TMR and throughput. The proposed CAM requires lesser number of transistors due to the compact XNOR operation enabled by the ME XNOR device, resulting in an area-efficient as well as energy-efficient CAM.

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